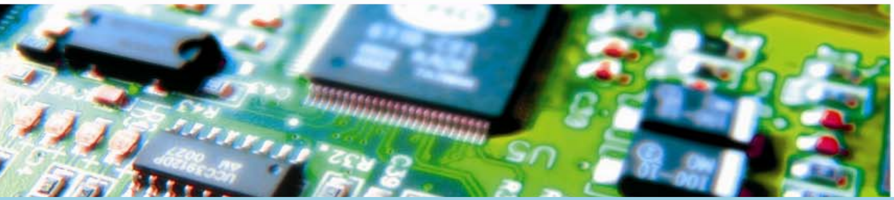

XtremeDSP Spartan-3A DSP Development Board

Technical Reference Guide

September, 2007

Revision history

Revision	Date	Comments
0.1	June, 2007	Preliminary version.
0.2	July, 2007	Added appendix 1.
0.3	July, 2007	Updated version for final review.
1.0	August, 2007	• Updated FMC information • Updated support information • Adjusted page numbering to meet specifications. • FPGA pinout for DDR2 inteface added • FPGA pinout for USB/System ACE inteface added

1.1	September, 2007	• Known issues section added
		  • Limitation of DDR2 clock rate to 133 MHz
		  • Soft Touch connector not compliant with Agilent probes
		  • FMC connector is in violation of some rules of the standard

To ensure the accuracy of the information contained herein, particular attention was given to usage in preparing this document. It corresponds to the product version manufactured prior to the date appearing on the title page. There may be differences between the document and the product, if the product was modified after the production of the document.

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Version 1.1
First edition, August, 2007

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Introduction

Congratulations on the purchase of the XtremeDSP Spartan-3A DSP Development Board.

Outstanding features and potential applications

The XtremeDSP Spartan-3A DSP Development Board uses, as its name implies, the new Spartan-3A DSP series of FPGAs from the Xilinx XtremeDSP product line. These devices offer developers great flexibility, a wide range of peripherals, and a cost-efficient solution to accelerate the development of new products. It is ideally suited for consumer-oriented wireless and multimedia video applications where cost-effective solutions are essential.

Document organization

This document is organized as follows:

Hardware overview presents the major hardware elements of the XtremeDSP Spartan-3A DSP Development Board, including connectors and various other components.

Configuration options presents the methods of configuring the XtremeDSP Spartan-3A DSP Development Board.

Known issues introduces the issues remaining with the XtremeDSP Spartan-3A DSP Development Board at the time of release.

Specifications outlines the major specifications of the XtremeDSP Spartan-3A DSP Development Board.

Conventions

In a procedure containing several steps, the operations that the user has to execute are numbered (*1*, *2*, *3*…). The diamond (♦) is used to indicate a procedure containing only one step, or secondary steps. Lowercase letters (*a*, *b*, *c*…) can also be used to indicate secondary steps in a complex procedure.

The abbreviation *NC* is used to indicate no connection.

Capitals are used to identify any term marked as is on an instrument, such as the names of connectors, buttons, indicator lights, etc. Capitals are also used to identify key names of the computer keyboard.

All terms used in software, such as the names of menus, commands, dialog boxes, text boxes, and options, are presented in **bold** font style.

The abbreviation *N/A* is used to indicate something that is not applicable or not available at the time of press.

Note
The screen captures in this document are taken from the software version available at the time of press. For this reason, they may differ slightly from what appears on your screen, depending on the software version that you are using. Furthermore, the screen captures may differ from what appears on your screen if you use different appearance settings.

Additional support resources

All the necessary information regarding the XtremeDSP Spartan-3A DSP Development Board is available on the Xilinx Web site at **www.xilinx.com/s3adsp_db**.

Xilinx is firmly committed to providing the highest level of customer service and product support. If you experience any difficulties when using the XtremeDSP Spartan-3A DSP Development Board or if it fails to operate as described, we suggest that you first consult the present document, then, if you are still in need of assistance, you can visit the Xilinx Web site and search the database of silicon and software questions and answers, or open a technical support case in WebCase at **www.xilinx.com/support**.

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Hardware overview

This chapter presents an overview the XtremeDSP Spartan-3A DSP Development Board by describing its parts and functions.

XtremeDSP Spartan-3A DSP Development Board block diagram

The XtremeDSP Spartan-3A DSP Development Board can be represented by the following block diagram:

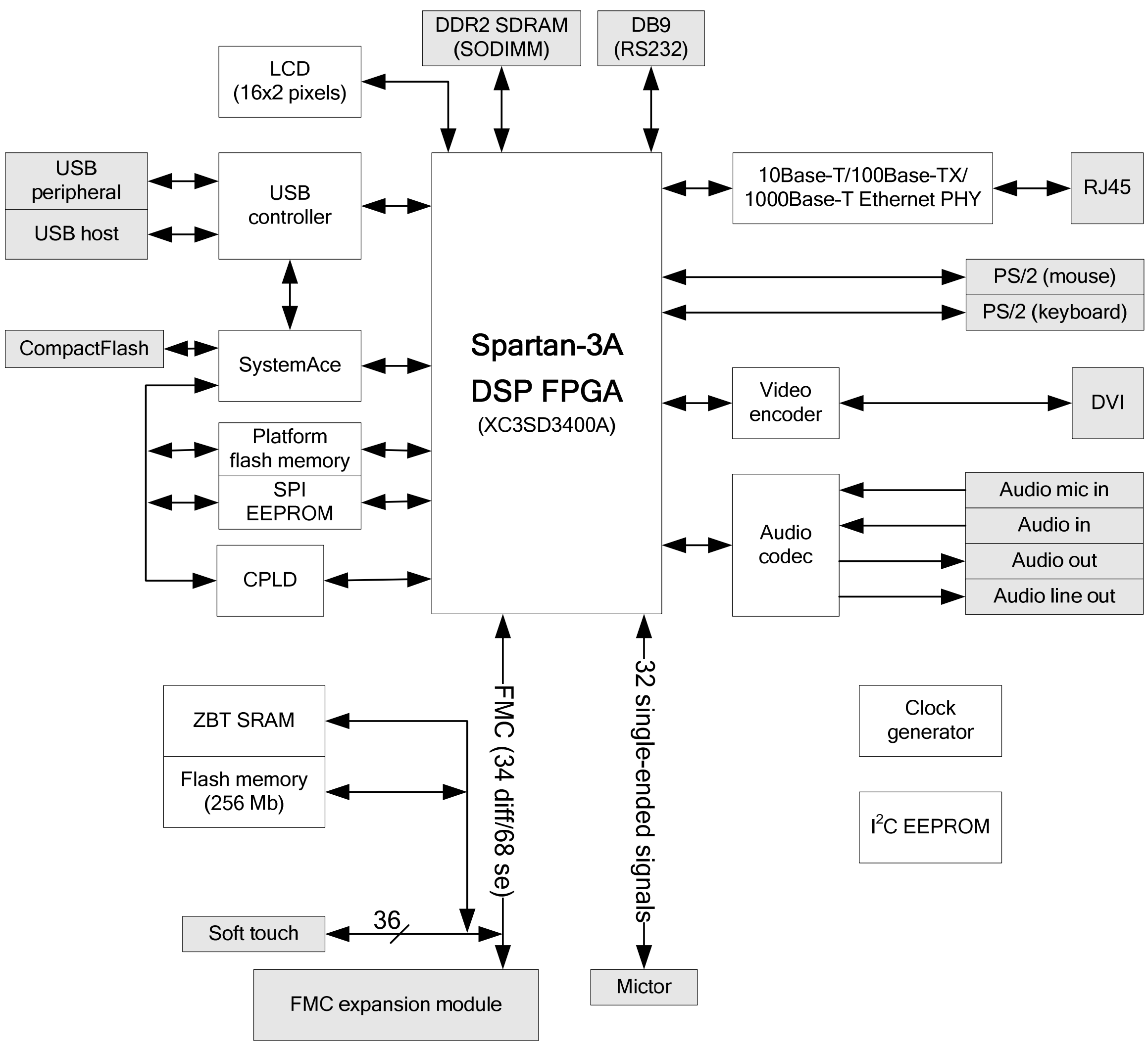

Figure 1 XtremeDSP Spartan-3A DSP Development Board block diagram

XtremeDSP Spartan-3A DSP Development Board parts and functions

Physically, the XtremeDSP Spartan-3A DSP Development Board is laid out as follows:

Top

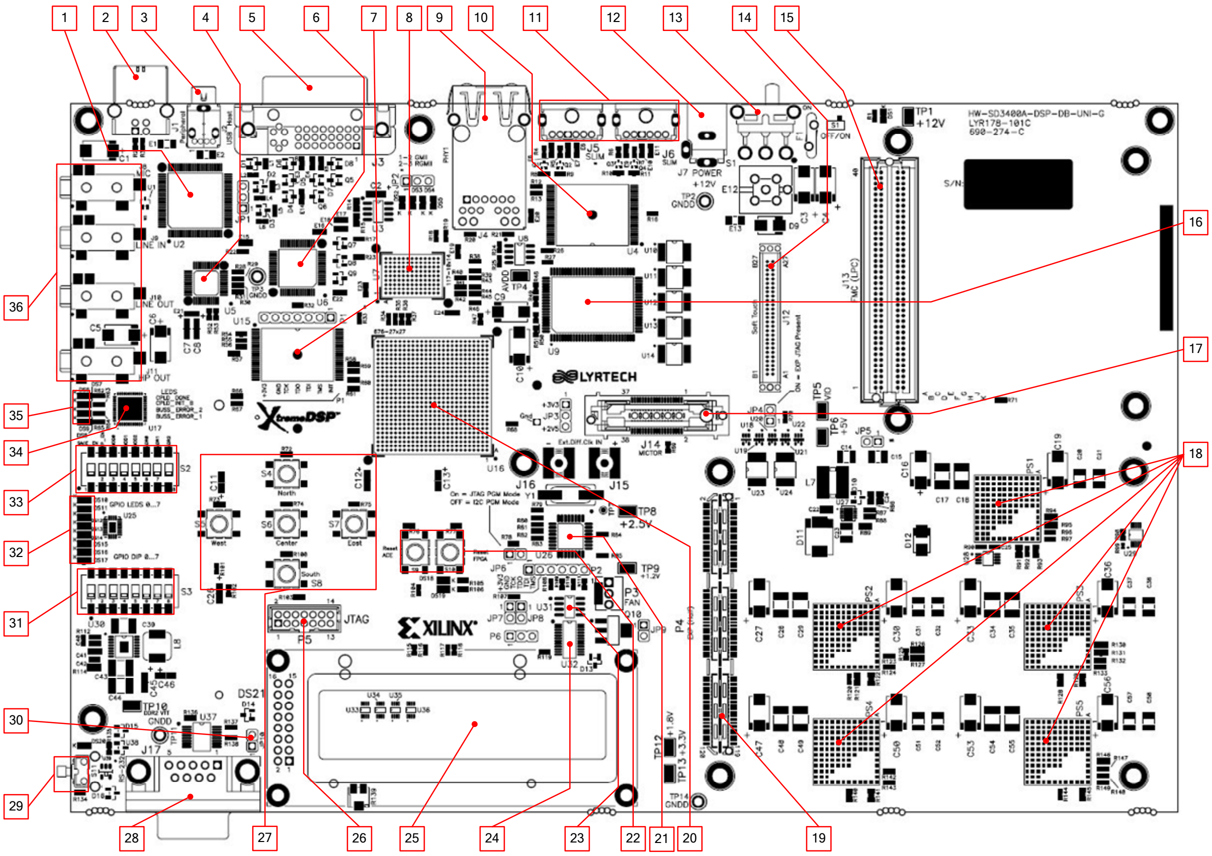

Figure 2 XtremeDSP Spartan-3A DSP Development Board top view

1. **USB controller**

   A Cypress CY7C67300 embedded USB host controller provides Hi-speed USB connectivity for the board. The USB controller supports host and peripheral modes of operation (see 2 and 3). The USB controller also has two serial interface engines (SIE) that can be used independently. SIE1 is connected to the USB host port (3). SIE2 is connected to the USB peripheral port (2).

   The USB controller is equipped with an internal microprocessor to assist in processing USB commands. The firmware for this processor may be stored in its dedicated I2C EEPROM (U41) or can be downloaded from a host computer through the USB peripheral port (below). Jumper JP1 can be installed (shorting pins 1 and 2) to prevent the USB controller from executing firmware stored in the I^2C EEPROM.

   The FPGA pins used for the USB interface are shared with the System ACE interface. See the FPGA pinout in the table below.

Table 1 FPGA USB/System ACE interface pinout

FPGA pin	Description	FPGA pin	Description
AE13	sysace_clk_in (System ACE only)	AD21	sace_usb_a_1
AE23	sace_mpce (System ACE only)	AA17	sace_usb_a_2
AA18	sysace_mpirq (System ACE only)	AE21	sace_usb_a_3
W17	usb_csn (USB only)	V16	sace_usb_a_4
AD22	usb_hpi_int (USB only)	AC20	sace_usb_a_5
AC21	sace_usb_oen	AD20	sace_usb_a_6
V17	sace_usb_wen	U16	sace_usb_a_7
AF4	sace_usb_a_0	AF20	sace_usb_a_8
W9	sace_usb_a_1	AE20	sace_usb_a_9
Y9	sace_usb_a_2	AC19	sace_usb_a_10
AE3	sace_usb_a_3	AF19	sace_usb_a_11
AF3	sace_usb_a_4	AE19	sace_usb_a_12
V15	sace_usb_a_5	AD19	sace_usb_a_13
U15	sace_usb_a_6	AC16	sace_usb_a_14
Y17	sace_usb_a_0	AB16	sace_usb_a_15

2. **USB peripheral port**

   Type B connector. Used to connect peripheral USB devices to the XtremeDSP Spartan-3A DSP Development Board.

3. **USB host port**

   Type A connector. Used to connect a host device to the XtremeDSP Spartan-3A DSP Development Board.

4. **AC'97 SoundaMAX codec**

   Analog Devices AD1981B. The device supports 16-bit stereo audio and sampling rates up to 48 kHz. The sampling rate for recording and playback may also be different.

   Note

   The codec's reset is shared with the reset signal of the flash memory devices. It is designed to be asserted when the development board is turned on or reset.

5. **DVI connector**

   The DVI connector is used to connect an external video monitor (DVI or VGA) to the XtremeDSP Spartan-3A DSP Development Board.

   Note

   The VGA monitor can be connected to the development board with a DVI-to-VGA adaptor (sold separately).

6. **Display controller device**

   The DVI circuitry uses a Chrontel CH7301C capable of 24-bit color and 1600 × 1200-pixel resolution. The display controller device drives the digital and analog signals to the DVI connector (5). The display controller device is controlled through the I^2C bus.

   The DVI connector supports the I^2C protocol, allowing the development board to read a monitor's configuration parameters. The parameters can then be read by the FPGA through the I^2C bus. See I^2C bus addressing for details.

7. Board flash PROM

Xilinx XCF32P. This flash PROM is used to program the development board's FPGA. The flash PROM can hold up to two distinct configuration images (up to four compressed configuration images) that can be accessed through the configuration DIP switches. You must use the same configuration DIP switches to configure the FPGA from the platform flash PROM. See 33 for details.

8. Ethernet PHY

Marvell Alaska 88E1111 PHY device. This PHY supports 10Base-T, 100Base-TX, and 1000Base-T (Gigabit) Ethernet. The PHY is connected to the board's Ethernet connector (9). The Ethernet PHY is initialized under its default configuration when the development board is turned on or reset. Jumper JP2 selects whether the PHY's default is RGMII mode (pins 2-3) or GMII mode (pins 1-2). The table below outlines the default configuration of the Ethernet PHY. You can modify this configuration through software.

Table 2 Ethernet PHY default configuration

Configuration pin	Board connection	Bit 2	Bit 1	Bit 0
CONFIG0	V_{cc} 2.5 V	PHYADR[2] = 1	PHYADR[1] = 1	PHYADR[0] = 1
CONFIG1	Ground	ENA_PAUSE = 0	PHYADR[4] = 0	PHYADR[3] = 0
CONFIG2	V_{cc} 2.5 V	ANEG[3] = 1	ANEG[2] = 1	ANEG[1] = 1
CONFIG3	V_{cc} 2.5 V	ANEG[0] = 1	ENA_XC = 1	DIS_125 = 1
CONFIG4	V_{cc} 2.5 V or LED_DUPLEX	HCWCFG_MODE[2] = 0 or 1	HCWCFG_MODE[1] = 1	HCWCFG_MODE[0] = 1
CONFIG5	V_{cc} 2.5 V	DIS_FC = 1	DIS_SLEEP = 1	HCWCFG_MODE[3] = 1
CONFIG6	LED_RX	SEL_BDT = 0	INT_POL = 1	75 Ω/50 Ω = 0

9. Ethernet port

10Base-T, 100Base-TX, and 1000Base-T (Gigabit) Ethernet port. Connected to the Ethernet PHY (8).

10. Flash memory

Intel StrataFlash embedded memory JS28F256P30B95. Provides the development board with 32-MB flash memory. This memory provides non-volatile storage for data, software, or bitstreams. The device is 16 bits wide. This flash memory can also be used to program the FPGA.

Note

The FMC module cannot be used when using the flash memory. Make sure that the FMC adjustable power supply is configured for 3.3 V to use the flash memory. See *FMC expansion connector* for instructions about how to properly configure the adjustable power supply.

The Flash memory shares the same data bus as the ZBT synchronous SRAM (16).

11. PS/2 connectors

The XtremeDSP Spartan-3A DSP Development Board is equipped with two PS/2 connectors for a keyboard and mouse. Bidirectional level shifting transistors allow the FPGA's 1.8-V and 3.3-V I/O to interface with the 5-V I/O of the PS/2 connectors, which are powered directly from the 5-V power source of the development board. Connector J5 is used to connect a mouse, while connector J6 is used to connect a keyboard.

Note

Make sure that the power load of connected PS/2 devices does not overload the AC adapter of the development board.

12. Power connector

Center positive, 2.1-mm × 5.5-mm barrel-type plug. Used to connect the supplied AC adaptor.

13. Power switch

Allows you to turn the XtremeDSP Spartan-3A DSP Development Board on and off by controlling the 12-V supply of the board.

14. Soft Touch connector

The Soft Touch connector (J12) allows you to monitor signals between the FPGA and the FMC expansion connector.

Table 3 Soft Touch connector pin assignments

Soft Touch pin	FPGA pin	Description	Soft Touch pin	FPGA pin	Description
A1	H2	FMC_LA18_P	B1	M8	FMC_LA19_P
A2	NC	GND	B2	NC	GND
A3	H1	FMC_LA18_N	B3	M7	FMC_LA19_N
A4	J5	FMC_LA31_P	B4	K3	FMC_LA32_P
A5	NC	GND	B5	NC	GND
A6	J4	FMC_LA31_N	B6	K2	FMC_LA32_N
A7	L4	FMC_LA29_P	B7	K5	FMC_LA30_P
A8	NC	GND	B8	NC	GND
A9	L3	FMC_LA29_N	B9	K4	FMC_LA30_N
A10	P8	FMC_LA16_P	B10	L10	FMC_LA17_P
A11	NC	GND	B11	NC	GND
A12	P9	FMC_LA16_N	B12	L9	FMC_LA17_N
A13	U1	FMC_LA14_P	B13	R8	FMC_LA15_P
A14	NC	GND	B14	NC	GND
A15	U2	FMC_LA14_N	B15	R7	FMC_LA15_N
A16	M10	FMC_LA12_P	B16	K6	FMC_LA13_P
A17	NC	GND	B17	NC	GND
A18	M9	FMC_LA12_N	B18	L7	FMC_LA13_N
A19	T5	FMC_LA33_P	B19	V1	FMC_LA11_P
A20	NC	GND	B20	NC	GND
A21	U4	FMC_LA33_N	B21	V2	FMC_LA11_N
A22	P7	FMC_LA24_P	B22	R5	FMC_LA25_P
A23	NC	GND	B23	NC	GND
A24	P6	FMC_LA24_N	B24	R6	FMC_LA25_N
A25	U5	FMC_LA26_P	B25	T10	FMC_LA27_P
A26	NC	GND	B26	NC	GND
A27	V5	FMC_LA26_N	B27	T9	FMC_LA27_N

15. FMC expansion connector

Samtec ASP-127796-01. The FMC expansion connector (J13) follows the VITA 57.1 FMC standard and is used in low pin count (LPC) format. See *FMC expansion connector* for details.

Note

The Flash Memory and ZBT synchronous SRAM cannot be used when using an FMC module. Make sure that the FMC adjustable power supply is configured for the voltage specified by the FMC module to use the FMC module properly. See *FMC expansion connector* for instructions about how to properly configure the adjustable power supply.

Table 4 FMC expansion connector pin assignments (1)

FMC pin	FPGA pin	Signal	FMC pin	FPGA pin	Signal
C1	NC	GND	D1	M2	PGC2M
C2	NC	DP0C2MP	D2	NC	GND
C3	NC	DP0C2MN	D3	NC	GND
C4	NC	GND	D4	NC	GBTCLK0M2CP
C5	NC	GND	D5	NC	GBTCLK0M2CN
C6	NC	DP0M2CP	D6	NC	GND
C7	NC	DP0M2CN	D7	NC	GND
C8	NC	GND	D8	G6	LA28PCC
C9	NC	GND	D9	H7	LA28NCC
C10	L4	LA29P	D10	NC	GND
C11	L3	LA29N	D11	D3	LA00P
C12	NC	GND	D12	E4	LA00N
C13	NC	GND	D13	NC	GND
C14	K5	LA30P	D14	E3	LA01P
C15	K4	LA30N	D15	F4	LA01N
C16	NC	GND	D16	NC	GND
C17	NC	GND	D17	K7	LA02P
C18	J5	LA31P	D18	J6	LA02N
C19	J4	LA31N	D19	NC	GND
C20	NC	GND	D20	M5	LA03P
C21	NC	GND	D21	M6	LA03N
C22	K3	LA32P	D22	NC	GND
C23	K2	LA32N	D23	N5	LA04P
C24	NC	GND	D24	N4	LA04N
C25	NC	GND	D25	NC	GND
C26	T5	LA33P	D26	N1	LA05P
C27	U4	LA33N	D27	N2	LA05N
C28	NC	GND	D28	NC	GND
C29	NC	GND	D29	A25	TCK
C30	AF23	SCL	D30	E23	TDI
C31	AE25	SDA	D31	NC	TDO
C32	NC	GND	D32	NC	3P3VAUX
C33	NC	GND	D33	D4	TMS
C34	NC	GA0 (ground)	D34	NC	TRSTL
C35	NC	12P0V	D35	NC	GA1 (gnd)
C36	NC	GND	D36	NC	3P3V

FMC pin	FPGA pin	Signal	FMC pin	FPGA pin	Signal
C37	NC	12P0V	D37	NC	GND
C38	NC	GND	D38	NC	3P3V
C39	NC	3P3V	D39	NC	GND
C40	NC	GND	D40	NC	3P3V

Table 5 FMC expansion connector pin assignments (2)

FMC pin	FPGA pin	Signal	FMC pin	FPGA pin	Signal
G1	NC	GND	H1	NC	VREFAM2C
G2	T3	CLK0C2MP	H2	G1	PRSNTM2CL
G3	T4	CLK0C2MN	H3	NC	GND
G4	NC	GND	H4	U3	CLK0M2CP
G5	NC	GND	H5	V4	CLK0M2CN
G6	L10	LA17P	H6	NC	GND
G7	L9	LA17N	H7	F5	LA06P
G8	NC	GND	H8	G4	LA06N
G9	H2	LA18P	H9	NC	GND
G10	H1	LA18N	H10	B2	LA07P
G11	NC	GND	H11	B1	LA07N
G12	M8	LA19P	H12	NC	GND
G13	M7	LA19N	H13	E1	LA08P
G14	NC	GND	H14	F2	LA08N
G15	J7	LA20P	H15	NC	GND
G16	H6	LA20N	H16	J8	LA09P
G17	NC	GND	H17	J9	LA09N
G18	K9	LA21P	H18	NC	GND
G19	K8	LA21N	H19	G3	LA10P
G20	NC	GND	H20	F3	LA10N
G21	M4	LA22P	H21	NC	GND
G22	M3	LA22N	H22	V1	LA11P
G23	NC	GND	H23	V2	LA11N
G24	N6	LA23P	H24	NC	GND
G25	N7	LA23N	H25	M10	LA12P
G26	NC	GND	H26	M9	LA12N
G27	P7	LA24P	H27	NC	GND
G28	P6	LA24N	H28	K6	LA13P
G29	NC	GND	H29	L7	LA13N
G30	R5	LA25P	H30	NC	GND
G31	R6	LA25N	H31	U1	LA14P

FMC pin	FPGA pin	Signal	FMC pin	FPGA pin	Signal
G32	NC	GND	H32	U2	LA14N
G33	U5	LA26P	H33	NC	GND
G34	V5	LA26N	H34	R8	LA15P
G35	NC	GND	H35	R7	LA15N
G36	T10	LA27P	H36	NC	GND
G37	T9	LA27N	H37	P8	LA16P
G38	NC	GND	H38	P9	LA16N
G39	NC	VADJ	H39	NC	GND
G40	NC	GND	H40	NC	VADJ

16. ZBT synchronous SRAM

ISSI IS61NLP25636A-200TQL. The ZBT synchronous SRAM is high-speed, low-latency external memory for the FPGA. The memory is organized as 256 K × 36 bits, providing a 32-bit data bus supporting four parity bits.

Note

The FMC module cannot be used when using the ZBT synchronous SRAM. Make sure that the FMC adjustable power supply is configured for 3.3 V to use the memory. See *FMC expansion connector* for instructions about how to properly configure the adjustable power supply.

The ZBT synchronous SRAM shares the same data bus as the flash memory (10).

17. Mictor

The mictor (J14) allows you to monitor up to 32 single-ended signals from the FPGA.

Table 6 Mictor pin assignments

Mictor pin	FPGA pin	Description	Mictor pin	FPGA pin	Description
1	NC	NC	2	NC	NC
3	NC	GND	4	NC	NC
5	A12	SE_CLK_IN	6	D13	SE_CLK_OUT
7	C10	SE_IO_9	8	B7	SE_IO_17
9	D10	SE_IO_11	10	B6	SE_IO_19
11	A9	SE_IO_7	12	NC	3.3V
13	B9	SE_IO_5	14	A4	SE_IO_21
15	B8	SE_IO_13	16	G9	SE_IO_23
17	A8	SE_IO_15	18	B4	SE_IO_25
19	C8	SE_IO_3	20	G10	SE_IO_27
21	C7	SE_IO_1	22	B3	SE_IO_28
23	K12	SE_IO_0	24	F7	SE_IO_29
25	G12	SE_IO_2	26	C6	SE_IO_16
27	K11	SE_IO_4	28	E7	SE_IO_18
29	H9	SE_IO_6	30	C5	SE_IO_20
31	J12	SE_IO_8	32	E10	SE_IO_22
33	H10	SE_IO_10	34	D9	SE_IO_24
35	J11	SE_IO_12	36	D6	SE_IO_26

Mictor pin	FPGA pin	Description	Mictor pin	FPGA pin	Description
37	H12	SE_IO_14	38	D8	SE_IO_30
39	NC	GND	40	NC	GND
41	NC	GND	42	NC	GND
43	NC	GND			

18. Power supply devices

The power supply circuitry of the XtremeDSP Spartan-3A DSP Development Board generates 0.9 V, 1.2 V, 1.8 V, 2.5 V, 3.3 V, and 5 V, as well as one adjustable voltage to power the components of the board. The 1.2 V (PS3), 1.8 V (PS5), 2.5 V (PS2), 3.3 V (PS4), and adjustable (PS1) supplies are driven by Linear Technology LTM4601 switching power regulators. The regulators are driven by a 753-kHz clock, making them run synchronously and reducing noise caused by beat frequencies. The clocks sent to each regulator are out of phase to reduce reflected noise at the input.

The adjustable device is user-configurable through the FPGA and is used for the VCCIO of the FPGA bank connected to the FMC expansion connector. When no FMC expansion module is present, the output voltage of PS1 should be set to 3.3 V with the I^2C bus interface to configure the digital potentiometer (U28). See *I^2C bus addressing* for details.

The diagram in Figure 3 illustrates the power supply architecture and maximum current handling by each supply. The typical operating currents are significantly below the maximum capacity. The XtremeDSP Spartan-3A DSP Development Board is normally shipped with a 60-W power supply, which should be suitable for most applications.

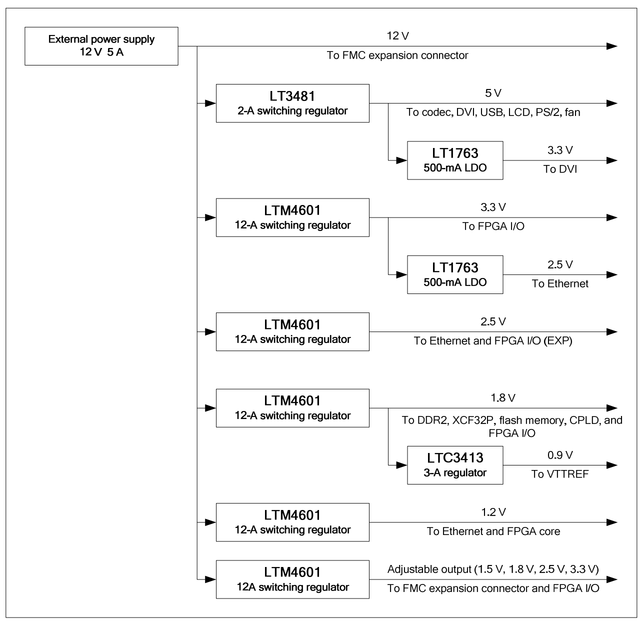

Figure 3 XtremeDSP Spartan-3A DSP Development Board power supply diagram

19. Expansion connector

This expansion connector is not used by the XtremeDSP Spartan-3A DSP Development Board.

20. FPGA

XC3SD3400A-4FGG676C Xilinx Spartan-3A DSP FPGA. The board supports configuration in several modes: JTAG, master serial, slave serial, master SelectMAP, slave SelectMAP, byte-wide peripheral interface (BPI) up, BPI down, and SPI modes. See *Configuration options* for details.

The FPGA is also equipped with four I/O banks. The I/O voltage applied to each bank is summarized below.

Table 7 FPGA I/O bank voltage rail

FPGA bank	I/O voltage rail
0	Adjustable (2.5 V or 3.3 V)
1	1.8 V
2	3.3 V
3	Adjustable (1.5 V, 1.8 V, 2.5 V, or 3.3 V)

21. Clock generator

IDT IDT5V9885PFGI. The clock generator is used to generate different clocks on the XtremeDSP Spartan-3A DSP Development Board. The following table summarizes the default settings of output clocks. The clock generator can be programmed through the I^{2}C interface. See *I^{2}C bus addressing* for details.

Table 8 Clock generator default settings

Clock output	Default frequency	Clock usage
1	25 MHz	Ethernet PHY clock.
2	14.31818 MHz	Audio codec clock.
3	12 MHz	USB clock.
4_P	33 MHz	System ACE clock.
4_N	33 MHz	FPGA clock (FPGA pin AE13).
5_P	200 MHz	FPGA differential clock P (FPGA pin AA13).
5_N	200 MHz	FPGA differential clock N (FPGA pin Y13).
6	27 MHz	FPGA clock (FPGA pin AF13).

22. Program and reset buttons

Button S10 is used to force the FPGA to be reprogrammed and button S9 is used to force the System ACE to reset.

23. 64-Kb I^{2}C EEPROM

The I^{2}C EEPROM 24LC64 can be used to store non-volatile data such as an Ethernet MAC address. The EEPROM is accessible through the I^{2}C bus. See *I^{2}C bus addressing* for details. The EEPROM write-protect is disabled on the board. I2C bus pull-up resistors are provided on the board.

The I^{2}C bus is extended to the FMC expansion connector so that the board can access additional I^{2}C devices and share the I^{2}C controller in the FPGA.

Table 9 I^{2}C FPGA pin assignments

I^{2}C signal	FPGA pin	Description
IIC_SCLK	AF23	I^{2}C clock
IIC_SDAT	AE25	I^{2}C data

24. I²C fan controller and temperature/voltage monitor

Onboard temperature and voltage monitoring and control are handled by an Analog Devices ADT7476A device. This device is controlled through I²C (see *I²C bus addressing* for details) and can:

- Measure the voltage of the 5-V, 3.3-V, 1.8-V, and 1.0-V supplies
- Measure the FPGA temperature through the DXP/DXN pins on the FPGA
- Measure ambient temperature
- Read power good status signals from the 2.5-V linear regulators
- Provide PWM control of the fan speed
- Provide fan tachometer readings
- Generate interrupts/alarms based on readings

Connector P3 is a keyed three-pin fan header similar to the ones in computers. It is designed to support a 5-V DC fan. To bypass the fan controller device and operate the fan at full speed, you can use connector JP9.

Under high-power operating conditions, a heatsink and/or fan for the FPGA can be accommodated on the board (*e.g.*, Calgreg Electronics Smart-CLIP family of heatsink/fan assemblies). The XtremeDSP Spartan-3A DSP Development Board does not come with a heatsink and/or fan.

25. LCD

Hantronix HDM16216L-2-L30S, 16-character × 2-line resolution LCD to display text information. The data interface to the LCD is connected to the FPGA and supports only the 4-bit mode. Onboard level shifters are used to shift the voltage level between the FPGA and the LCD. The LCD is equipped with a connector that allows the LCD to be removed from the development board to gain access to the composnents below. Turning the potentiometer located below the LCD with a screwdriver allows you to adjust the image contrast of the LCD. The LCD is equipped with a backlight that can be turned off by removing jumper JP10.

Note

Take care not to scratch or otherwise damage the LCD.

26. JTAG header

The JTAG header (P5) allows programming devices and troubleshooting the FPGA. The JTAG port supports the Xilinx Parallel Cable III, Parallel Cable IV, or Platform USB cable products. Third-party configuration products might also be available. The JTAG chain can also be extended to the FMC expansion module when it is present. See *Configuration options* for details.

27. User-defined buttons

The functions of the five user-defined buttons are entirely up to you. The buttons are directly connected to the FPGA.

Table 10 User-defined button FPGA pin assignments

Button no.	FPGA pin	Description
S4	N25	GPIO_SW_NORTH
S5	N26	GPIO_SW_WEST
S6	Y26	GPIO_SW_CENTER
S7	N23	GPIO_SW_EAST
S8	P21	GPIO_SW_SOUTH

28. RS232 serial port

This DB9 connector allows the FPGA to communicate serial data to another device. The port is wired as a host device (DCE) and configured to operate at up to 115200 bauds. An interface device is used to shift the voltage level between FPGA and RS232 signals.

Table 11 Serial port FPGA pin assignments

DB9 pin	FPGA pin	Description
2	V14	TX
3	W15	RX

Note

The FPGA is only connected to the TX and RX data pins of the serial port. As such, other RS232 signals such as hardware flow-control signals are not used. Flow control should therefore be disabled when communicating with a computer.

29. General reset button

The general reset button is an active-low button used as a system or user reset.

Table 12 Reset connection

Button	FPGA Pin	Description
S11	Y16	PORESET

30. Configuration jumpers

10 configuration jumpers are present on the XtremeDSP Spartan-3A DSP Development Board. The following tables describes how to use them:

Table 13 Configuration jumpers

Jumper	Function	On	Off
JP1	Prevents the USB controller from running the firmware in the I^2C EEPROM.	1-2: Does not run the firmware from I^2C EEPROM.	Runs the firmware from the I^2C EEPROM (default)
JP2	Ethernet modes.	1-2: GMII (default) 2-3: RGMII	N/A
JP3	Unused expansion connector I/O bank voltage selection.	1-2: 3.3 V (default) 2-3: 2.5 V	N/A
JP4	Unused expansion connector JTAG presence detection.	JTAG presence detected	JTAG not detected (default)
JP5	FMC I/O bank voltage selection.	Voltage present a FPGA (default)	No voltage present at FPGA
JP6	Clock generator programming mode.	JTAG programming (default)	I^2C programming
JP7/JP8	System ACE failsafe mode.	Failsafe mode enabled when both jumpers are populated	Failsafe mode disabled when both jumpers are unpopulated
JP9	Fan controller bypass.	Fan controller bypassed	Fan controller is not bypassed (default)
JP10	LCD backlight control.	Backlight is on (default)	Backlight is off

31. User-defined DIP switches

Eight general-purpose, active-high DIP switches (S3) are connected to the user I/O pins of the FPGA.

Table 14 User-defined DIP switch FPGA pin assignments

Switch no.	FPGA pin	Description
1	R26	FPGA_DIP_SW0
2	R25	FPGA_DIP_SW1
3	T23	FPGA_DIP_SW2
4	R24	FPGA_DIP_SW3
5	T18	FPGA_DIP_SW4
6	R22	FPGA_DIP_SW5
7	R21	FPGA_DIP_SW6
8	R20	FPGA_DIP_SW7

32. User-defined LEDs

Eight general-purpose, active-high LEDs (DS10–DS17) are connected to the user I/O pins of the FPGA.

Table 15 User-defined LED FPGA pin assignments

LED no.	FPGA pin	Description
1 (DS10)	W23	GPIO_LED_0
2 (DS11)	V22	GPIO_LED_1
3 (DS12)	V25	GPIO_LED_2
4 (DS13)	V24	GPIO_LED_3
5 (DS14)	V23	GPIO_LED_4
6 (DS15)	U23	GPIO_LED_5
7 (DS16)	U22	GPIO_LED_6
8 (DS17)	T24	GPIO_LED_7

33. Configuration DIP switches

Eight configuration DIP switches (S2) allow you to configure the System ACE configuration address and the FPGA configuraiton mode. They also allow you to enable the fallback configuration of the board's System ACE configuration.

Table 16 Configuration DIP switch functions

Switch no.	Function	On position	Off position
8	System ACE Config address [2].	0	1
7	System ACE Config address [1].	0	1
6	Configuration address [0].	0	1
5	Config Mode [2] (see Table 17)	0	1
4	Config Mode [1] (see Table 17)	0	1
3	Config Mode [0] (see Table 17)	0	1
2	Board flash memory fallback	0 (Disabled)	1 (Enabled)

Switch no.	Function	On position	Off position
1	System ACE configuration When the System ACE configuration is enabled, the System ACE controller (on the bottom of the board) configures the FPGA from the CompactFlash card reader (on the bottom of the board) whenever a CompactFlash card is inserted in the reader or the *Reset ACE* button is depressed.	0 (Disabled)	1 (Enabled)

Table 17 Configuration modes

Configuration mode	Configuration source	Mode [2]	Mode [1]	Mode [0]
MASTER SERIAL	CONFIG FROM XCF32P FLASH	0	0	0
MASTER SPI	CONFIG FROM SPI EEPROM	0	0	1
MASTER BPI-UP	NOT SUPPORTED	0	1	0
MASTER BPI-DOWN	NOT SUPPORTED	0	1	1
MASTER SELECTMAP	CONFIG FROM XCF32P FLASH	1	0	0
JTAG	CONFIG FROM SYSTEMACE	1	0	1
SLAVE SELECTMAP	CONFIG FROM XCF32P FLASH	1	1	0
SLAVE SERIAL	CONFIG FROM XCF32P FLASH	1	1	1

34. CPLD

Xilinx XC2C64A CoolRunner-II. This device is designed for high-performance and low-power applications. The CPLD is used to configure the XtremeDSP Spartan-3A DSP Development Board and to provide statuses through the status LEDs (below).

35. Status LEDs

The status LEDs are driven by the CPLD to provide statuses on the XtremeDSP Spartan-3A DSP Development Board.

Table 18 Status LED signals

LED	Signal	Description
DS6	DONE	Status of the FPGA DONE signal
DS7	INIT	Satus of the FPGA INIT signal
DS8	BUS_ERROR_2	Not used
DS9	BUS_ERROR_1	Not used

36. Audio input output connectors

Microphone, line in, line out, and headphones connectors. All the connectors are stereo except the microphone connector.

Table 19 Audio connectors

Connector	Function
J8	Microphone — In
J9	Analog line — In
J10	Analog line — Out
J11	Headphones — Out

Bottom

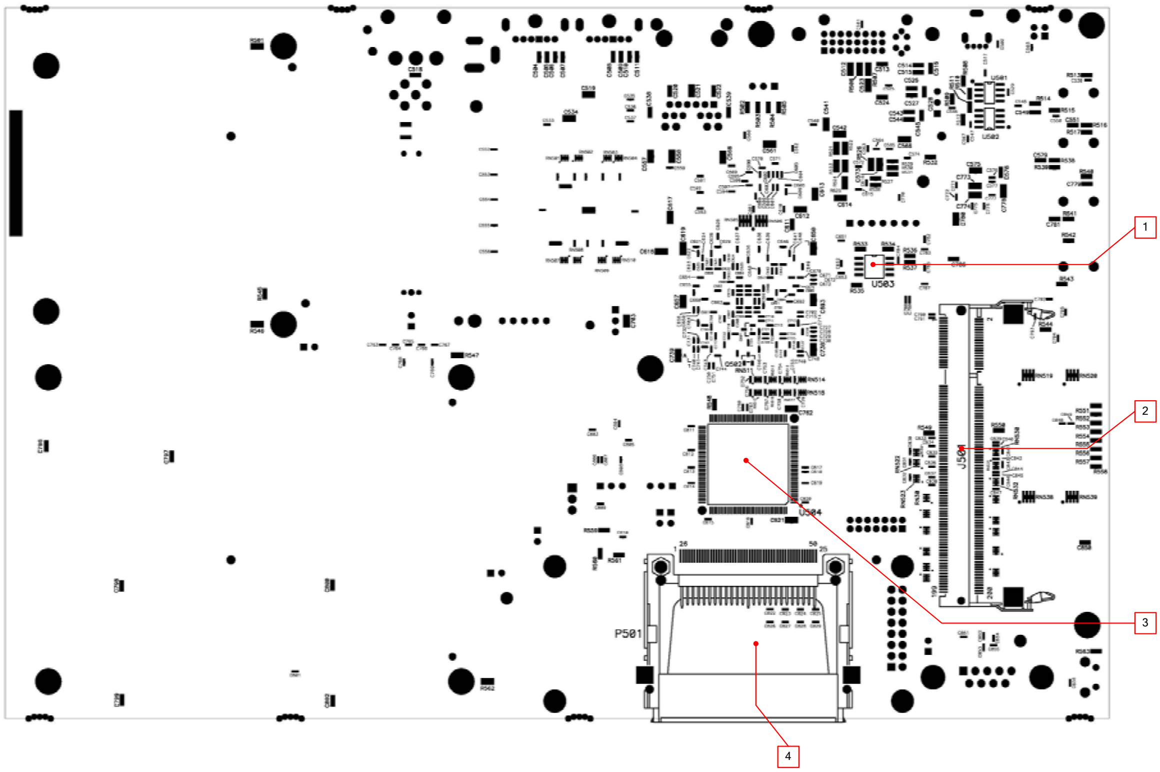

Figure 4 XtremeDSP Spartan-3A DSP Development Board bottom view

1. **SPI EEPROM**

   ST Microelectronics M25P16 16-Mb SPI EEPROM. The device can be used to configure the FPGA or to hold user data. See *Configuration options* for details.

2. **DDR2 SDRAM**

   The XtremeDSP Spartan-3A DSP Development Board is equipped with a single-rank, unregistered 512-MB DDR2 SDRAM. The DDR2 SDRAM isususlly a Micron MT8HTF6464HY-53E or similar. Serial presence detection (SPD) through an I^2C interface to the memory is also supported by the FPGA. See *DDR2 memory* for details.

   See the FPGA pinout used for the DDR2 interface on Table 20.

   Notes

   - Only half the the available memory of the DDR2 SDRAM (*i.e.* 256 MB) is available because of certain limitations.
   - The XtremeDSP Spartan-3A DSP Development Board is only tested for DDR2 SDRAM operation at a data rate of 266 MHz (133 MHz clock rate). Using faster data rates is possible, but untested and not garanteed.

Table 20 FPGA DDR2 interface pinout

FPGA pin	Description	FPGA pin	Description
AA25	DDR2_A_0	N24	DDR2_0_DQ_0
AA22	DDR2_A_1	M26	DDR2_0_DQ_1
AB26	DDR2_A_2	M25	DDR2_0_DQ_2
Y21	DDR2_A_3	P23	DDR2_0_DQ_3
AC24	DDR2_A_4	N21	DDR2_0_DQ_4
AA24	DDR2_A_5	P22	DDR2_0_DQ_5
AD26	DDR2_A_6	P20	DDR2_0_DQ_6
AE26	DDR2_A_7	P26	DDR2_0_DQ_7
AB23	DDR2_A_8	M20	DDR2_0_DQ_8
AC25	DDR2_A_9	L24	DDR2_0_DQ_9
W21	DDR2_A_10	J25	DDR2_0_DQ_10
AD25	DDR2_A_11	J26	DDR2_0_DQ_11
AC23	DDR2_A_12	N17	DDR2_0_DQ_12
V19	DDR2_A_13	N20	DDR2_0_DQ_13
V21	DDR2_0_BA_0	M23	DDR2_0_DQ_14
AA23	DDR2_0_BA_1	M21	DDR2_0_DQ_15
AC26	DDR2_0_BA_2	G24	DDR2_0_DQ_16
U20	DDR2_0_CAS_B	G23	DDR2_0_DQ_17
U18	DDR2_0_CK0_N	K22	DDR2_0_DQ_18
U19	DDR2_0_CK0_P	M19	DDR2_0_DQ_19
D26	DDR2_0_CK1_N	F24	DDR2_0_DQ_20
E26	DDR2_0_CK1_P	K23	DDR2_0_DQ_21
Y23	DDR2_0_CKE	K21	DDR2_0_DQ_22
P25	DDR2_0_DM_0	L22	DDR2_0_DQ_23
N18	DDR2_0_DM_1	F23	DDR2_0_DQ_24
M22	DDR2_0_DM_2	E24	DDR2_0_DQ_25
M18	DDR2_0_DM_3	K20	DDR2_0_DQ_26
N19	DDR2_0_DQS0_N	L20	DDR2_0_DQ_27
P18	DDR2_0_DQS0_P	G22	DDR2_0_DQ_28
K26	DDR2_0_DQS1_N	F25	DDR2_0_DQ_29
K25	DDR2_0_DQS1_P	K18	DDR2_0_DQ_30
J22	DDR2_0_DQS2_N	K19	DDR2_0_DQ_31
J23	DDR2_0_DQS2_P	C25	DDR2_LOOP_OUT
L17	DDR2_0_DQS3_N	H24	DDR2_LOOP_IN
L18	DDR2_0_DQS3_P	W20	DDR2_0_S0
Y22	DDR2_0_ODT_0	V18	DDR2_0_S1
U21	DDR2_0_ODT_1	T20	DDR2_0_WE_B
Y20	DDR2_0_RAS_B		

3. System ACE controller

The Xilinx System ACE controller allows a type I CompactFlash card to program the FPGA through the JTAG port. The System ACEc controller supports up to eight configuration images on a single CompactFlash card. The configuration address DIP switches (33 on the top of the board) allow you to select what configuration image to use.

System ACE error and status LEDs indicate the operational state of the System ACE controller:

- The DS19 LED blinks red to indicate that no CompactFlash card is present.
- The DS19 LED lights red to indicate an error during configuration.
- The DS18 LED blinks green to indicate an ongoing configuration operation.
- The DS18 LED lights green to indicate a successful download.

Every time that a CompactFlash card is inserted in the CompactFlash reader, a configuration operation is initiated. Pressing the System ACE reset button (S9) reprograms the FPGA.

The FPGA pins used for the USB interface are shared with the System ACE interface. See the FPGA pinout on Table 1.

Note

Configuration with the System ACE controller is enabled with the configuration DIP switches.

The board also features a System ACE failsafe mode. Under this mode, if the System ACE controller detects a failed configuration attempt, it automatically restarts under a predefined configuration image. The failsafe mode is enabled by inserting two jumpers across JP7 and JP8 (horizontally or vertically).

Caution

Exercise caution when handling a CompactFlash card in the vicinity of the board, as contact between the card’s metallic parts and board components could create short-circuits.

The System ACE MPU port is connected to the FPGA. This connection allows the FPGA to use the System ACE controller to reconfigure the system or access the CompactFlash card as a generic FAT file system. The data bus for the System ACE MPU port is shared with the USB controller.

4. CompactFlash reader

The CompactFlash reader is used as an interface point between the XtremeDSP Spartan-3A DSP Development Board and a CompactFlash card. The CompactFlash card used is generally a Lexar Media 256-MB module

FMC expansion connector

The FMC expansion connector (J13) follows the VITA 57.1 FMC standard (standard to be released at a later date) and it is used in low-pin-count (LPC) format. The XtremeDSP Spartan-3A DSP Development Board was designed with a preliminary version of the standard.

When an FMC mezzanine module is intended to be used, the FPGA should access the FMC mezzanine module's I^2C EEPROM to read the board's information. This information allows the FPGA to set the appropriate I/O voltages to the FPGA I/Os connected to the FMC expansion connector. The way the board information will be stored in the FMC mezzanine I^2C EEPROM is not defined at this time. A work group is currently developing the Vita-57.2 standard. The standard should be released soon.

To set the appropriate voltage on the FMC connector, an I^2C digital pot must be set to a specific value. The value should be written to the volatile register of the digital pot. This register is located at address 0x00 if address 0x02 is set to 0x80.

The following steps are used in configuring the digital pot to the following voltages:

Vout = 1.5 V

1. Configure register 0x2 to value 0x80
2. Configure register 0x0 to value 0x8A

Vout = 1.8 V

1. Configure register 0x2 to value 0x80
2. Configure register 0x0 to value 0x57

Vout= 2.5 V

1. Configure register 0x2 to value 0x80
2. Configure register 0x0 to value 0x1E

Vout = 3.3 V

1. Configure register 0x2 to value 0x80
2. Configure register 0x0 to value 0x00

DDR2 memory

DDR2 memory expansion

The SODIMM connector allows you to install DDR2 SODIMM modules with more memory because higher order addresses and chip select signals are also routed from the SODIMM connector to the FPGA. However, a permanent limitation is that only the first 32 bits of data are routed to the FPGA.

DDR2 clock signal

Two, matched length pairs of DDR2 clock signals are broadcast from the FPGA to the SODIMM connector. The FPGA design is responsible for driving the two clock pairs at a low skew. The delay on the clock traces is designed to match the delay of the other DDR2 control signals.

DDR2 signaling

All DDR2 control signals are terminated through 47-Ω resistors to a 0.9-V VTT reference voltage. The DDR2 interface of the FPGA supports SSTL18 signaling and all the DDR2 signals are controlled impedances. The DDR2 data, mask, and strobe signals are of matched length within byte groups. On die termination (ODT) is available and better performance can be achieved when used by the memory controller.

MIG compatibility

Since MIG doesn't directly generate compatible design for the XtremeDSP Spartan-3A DSP Development Board at this time, the used design can't be called MIG-compatible. However, the board can be used with a modified design from MIG.

I^{2}C bus addressing

The XtremeDSP Spartan-3A DSP Development Board uses an I^{2}C bus to interface different devices to the FPGA. The following table shows the slave addresses of these devices:

Table 21 I^{2}C slave device addresses

Device	A7	A6	A5	A4	A3	A2	A1	A0
Fan controller	0	1	0	1	1	0	0	R/W
Video encoder	1	1	1	0	1	1	0	R/W
Digital potentiometer for FMC power supply adjustment	0	1	0	1	0	0	0	R/W
I^{2}C EEPROM	1	0	1	0	1	0	0	R/W
Clock generator	1	1	0	1	0	1	0	R/W
FMC module I^{2}C EEPROM	1	0	1	0	X	0	0	R/W

Note

The FMC module's manufacturer supplies the value of A3.

Configuration options

The FPGA of the XtremeDSP Spartan-3A DSP Development Board can be configured by four major devices:

- Xilinx download cable (JTAG)
- System ACE controller (JTAG)
- Board flash memory
- SPI flash memory

The following section provides an overview of the possible ways the FPGA can be configured.

JTAG configuration

The FPGA, board's flash memory, and CPLD can all be configured through the JTAG port of the XtremeDSP Spartan-3A DSP Development Board. The JTAG chain of the board is illustrated below.

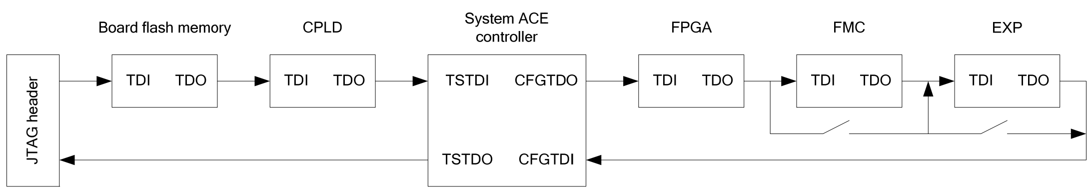

Figure 5 XtremeDSP Spartan-3A DSP Development Board JTAG chain

The chain starts at the JTAG header (see *XtremeDSP Spartan-3A DSP Development Board parts and functions*) and goes through the System ACE controller, the board flash memory, the FPGA, the CPLD and the FMC expansion connector. The chain bypasses the FMC expansion connector if there is no expansion module present. JP4 jumper must not be populated for appropriate JTAG operation.

The JTAG chain can be used to program the FPGA and access the FPGA for hardware and software troubelshooting.

The JTAG header's connection to the JTAG chain allows a host computer to transfer bitstreams to the FPGA using iMPACT from Xilinx. The JTAG header also allows such troubleshooting tools as ChipScope Pro to access the FPGA.

The System ACE controller can also program the FPGA through the JTAG port. By inserting a CompactFlash card in the CompactFlash reader (see *XtremeDSP Spartan-3A DSP Development Board parts and functions*), configuration information can be stored and programmed on the FPGA. The System ACE controller supports up to eight configuration images that can be selected using the three configuration address DIP switches (see *XtremeDSP Spartan-3A DSP Development Board parts and functions*). Under the control of the FPGA, the System ACE controller can be instructed use any of the eight configuration images.

The configuration mode should be set to 101 (ACE_CFGADDR0_IN (OFF), ACE_CFGADDR1_IN (ON), ACE_CFGADDR2_IN (OFF) and ACE_CFG_EN should be OFF to use System ACE configuration (see item 33, above).

When set correctly, the System ACE controller programs the FPGA upon power-up if a CompactFlash card is present or whenever a CompactFlash card is inserted. Pressing the System ACE reset button also causes the System ACE controller to program the FPGA if a CompactFlash card is present.

Board flash memory configuration

The board flash memory can also be used to program the FPGA. This memory can hold up to two configuration images (up to four with compression), selectable with the two least significant bits of the configuration address DIP switches (see *XtremeDSP Spartan-3A DSP Development Board parts and functions*).

The board is designed in such a way that the board flash memory can download bitstreams under master serial, slave serial, master SelectMAP (parallel), or slave SelectMAP (parallel) modes. Using iMPACT to program the memory, you can select which of the four modes to use in programming the FPGA. The configuration mode DIP switches on the board must match the programming method used by the memory (see item 33, above).

When correctly configured, the board flash memory programs the FPGA when the XtremeDSP Spartan-3A DSP Development Board is turned on or whenever the program button is depressed (see item 22, above).

SPI flash memory configuration

Data stored in the SPI flash memory can be used to program the FPGA. The configuration mode DIP switches must be set to *0 0 1* to configure the FPGA from the SPI flash memory (see item 33, above).

When correctly configured, the FPGA is programmed when the XtremeDSP Spartan-3A DSP Development Board is turned on or whenever the program button is depressed.

Specifications

This chapter outlines the technical specifications of the XtremeDSP Spartan-3A DSP Development Board.

Note
The specifications in this chapter are subject to change without notice.

General specifications

- Mass: 359.1 g
- Length: 254.0 mm
- Width: 165.1 mm
- Height: 40 mm (feet included)
- Feet: 15 mm
- Operating temperature range: 0ºC to 70ºC (non-condensing)
- Storage temperature range: –55ºC to 150ºC (non-condensing)

Maximum power consumption

- 6.84 W

Notes
- These power consumption specifications were calculated with a production test bitstream.
- The power consumptions outlined above may vary according to the FPGA load.

FPGA

- Model: Xilinx Spartan-3A DSP, XC3SD3400A-4FGG676C
- DSP Performance: 32 GMACS
- Maximum DSP frequency: 250 MHz
- Block RAM: 2,268 Kb
- Logic cells: 53,712
- Speed: 213 × 622+ Mbps LVDS pairs

Memory

- 256-MB DDR2 SDRAM
- 256-Mb flash memory
- 9-Mb ZBT SRAM
- 32-Mb board flash memory
- 16-Mb SPI EEPROM
- 512-MB CompactFlash

Connectors and interfaces

- RJ45 — 10Base-T, 100Base-TX, 1000Base-T Ethernet
- RS232 serial port
- System ACE Compact Flash
- JTAG programming interface
- Video (DVI/VGA) output
- Audio in (2×) — line and microphone
- Audio out (2×) — line and amplifier
- USB (2×) — host and peripheral
- LCD (2 × 16)
- CompactFlash connector
- GPIO DIP switch (8×), LED (8×), and buttons
- DDR2 SODIMM connector
- PS/2 (2×) — keyboard and mouse
- FMC LPC expansion connector
- Mictor trace port
- Soft Touch Pro

Known issues

The following is a list of the know issues regarding the XtremeDSP Spartan-3A DSP Development Board.

- The Soft Touch connector pin assignments do not comply with the Soft Touch standard from Agilent. No Soft Touch probe can be used with the XtremeDSP Spartan-3A DSP Development Board.
- The FMC connector used on the XtremeDSP Spartan-3A DSP Development Board does not **completely** comply with the latest FMC standard (as the standard is yet to be released). The following table lists the rules and recommendations violated on the XtremeDSP Spartan-3A DSP Development Board.

Table 22 FMC standard rule and recommendation violations

Rule/Recommendation	Violation
Rule 27	No available front panel on the XtremeDSP Spartan-3A DSP Development Board. The isolation between the chassis ground and digital ground is performed with a ferrite.
Rule 28	Standoffs adjacent to FMC connector or not connected to the chassis ground or digital ground.
Recommendation 7	LA17 and LA28 are not connected to clock-capable I/Os.
Recommendation 11	CLK0_M2C signals are not connected to dedicated clock pins.

- The DDR2 interface performance is limited to a clock rate of 133 MHz on the XtremeDSP Spartan-3A DSP Development Board.

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Appendix 1 Clock generator programming

The XtremeDSP Spartan-3A DSP Development Board features an Integrated Device Technology (IDT) 3.3-V EEPROM programmable clock generator that allows you to program the board's clocks. This appendix explains how to use the IDT software to generate a combination of clock frequencies and implement them onto the XtremeDSP Spartan-3A DSP Development Board with a Xilinx download cable and JTAG flying wires.

Installing the clock generator software

1. Visit the IDT Web site at this address **www1.idt.com/?genID=5V9885**.
2. To download the ZIP file of the program, in the **Related Documents** group at the bottom of the page, click **Programming Software**.
3. Unzip and install the software.
4. At some point, you may be prompted to install the Java Runtime Environment. Install it.
5. Follow the instructions on your screen to complete installation.

Generating an SVF file

When the IDT software is installed, use it to create an SVF file to program the clock chip of the XtremeDSP Spartan-3A DSP Development Board.

To start the IDT program

1. On the Windows **Start** menu, point to **IDT Programmable Clock Devices**, and then click **IDT Programmable Clock**.
2. When the program starts, click **5V9885**.

Figure 6 IDT Programmable Clock

To select I/O settings

1. Modify the input clock frequency from 20 MHz to 25 MHz so that it matches the clock input frequency of the XtremeDSP Spartan-3A DSP Development Board.
2. Click the **Detailed I/O**.

   The following window appears.

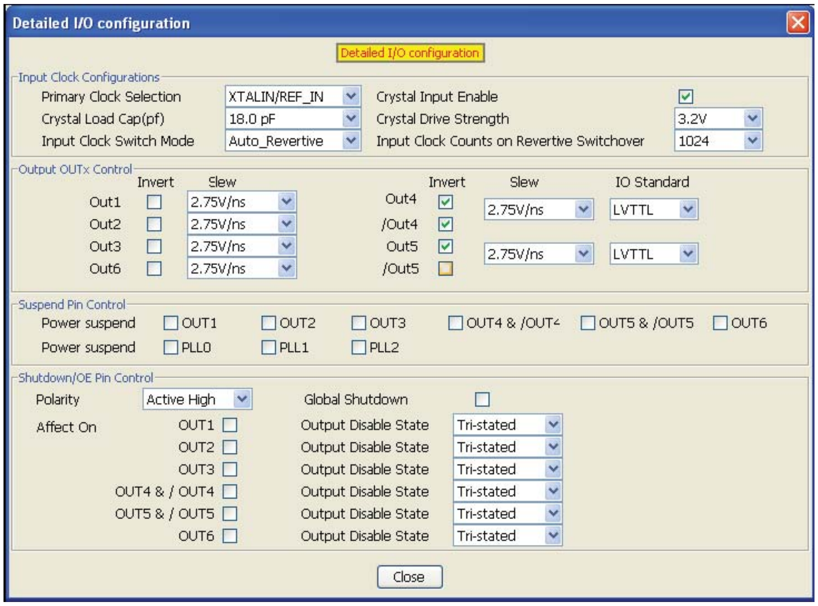

Figure 7 Detailed I/O configuration of the 5V9885

3. In the **Input Clock Configurations** group, select the **Crystal Input Enable** check box.
4. In the **Output OUTx Control** group, clear the **/Out5 Invert** check box.

   On the XtremeDSP Spartan-3A DSP Development Board, clock output 5 is usually used as a differential clock.
5. Click **Close**.
6. Under **Output Clock Frequencies**, type the clock output frequencies in the appropriate text boxes.
7. To calculate the register values necessary to produce the clock frequencies, click **Auto Calculate**.

   The **Auto Calculation Result** window appears.
8. Click **OK** to close the window.

   Under each text box where you typed a value, blue text indicates the frequencies to be produced. When you see a double dash (- -) instead of a numerical value, the software was unable to create this combination of clock frequencies. Modify the settings until all the clock outputs are numerical values.

   During startup, the chip loads its settings depending on the GIN input pins. By default, the software loads from the configuration-0 settings. The configuration used by the XtremeDSP Spartan-3A DSP Development Board requires some register modifications to function properly.

To selecting register settings

1. Click the **Register Settings** tab.
2. Copy the contents of the register in the left column to the register in the right column by matching the checkboxes. For example, the configuration in Table 23 requires that you copy the settings from register `0x8` to register `0xB`, then to copy the settings from register `0xC` to register `0xF`, and so on. Figure 8 presents how the contents are copied for registers `0x13`, `0x17`, `0x1B`, and `0x21`.

Table 23 Register configuration

Register address (Config 0)	Register address (XtremeDSP Spartan-3A DSP Development Board configuration)
0x8	0xB
0xC	0xF
0x10	0x13
0x14	0x17
0x18	0x1B
0x20	0x21
0x24	0x25
0x28	0x29
0x2C	0x2D
0x30	0x31
0x38	0x39
0x3C	0x3D
0x40	0x41
0x44	0x45
0x48	0x49

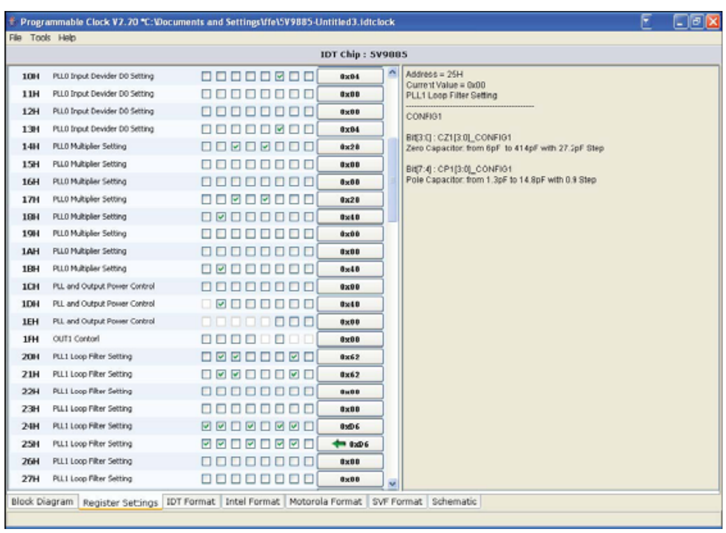

Figure 8 Assigning the register settings

3. On the **File** menu, click **Export SVF file**.
4. Type a name for the SVF file, and then click **OK**.

Downloading to the XtremeDSP Spartan-3A DSP Development Board

1. Connect a Xilinx download cable to the XtremeDSP Spartan-3A DSP Development Board.
2. To enable the JTAG programming mode, place a jumper on JP6.
3. On the Widnows **Start** menu, click **iMPACT**.
4. Select **Boundary Scan**.
5. Right-click the device and click **Assign New Configuration File** on the shortcut menu that appears.
6. Locate the SVF file (*sdsp_clock_setup.svf* as the example below), and then click **Open**.
7. Right-click the device and click **Execute XSVF/SVF** on the shortcut menu that appears.

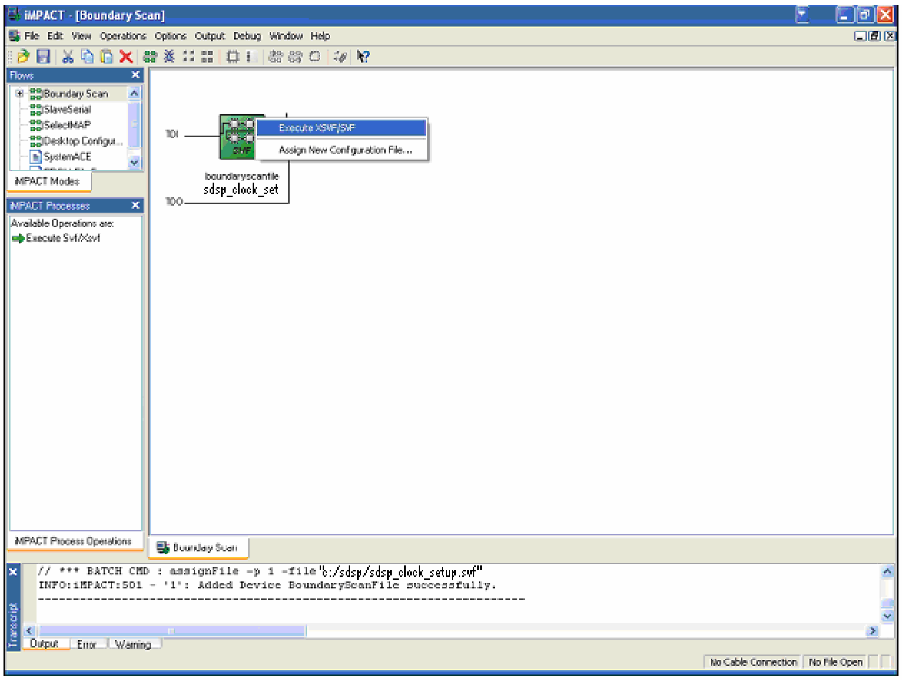

Figure 9 Programming the XtremeDSP Spartan-3A DSP Development Board with iMPACT

8. To complete programming the device, turn off the XtremeDSP Spartan-3A DSP Development Board, and then turn it on again.
9. Verify that the clock frequencies are correct.

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